

# STM32 CubeMX

## 1. Description

### 1.1. Project

Project Name	cube
Board Name	custom
Generated with:	STM32CubeMX 6.0.0
Date	11/07/2020

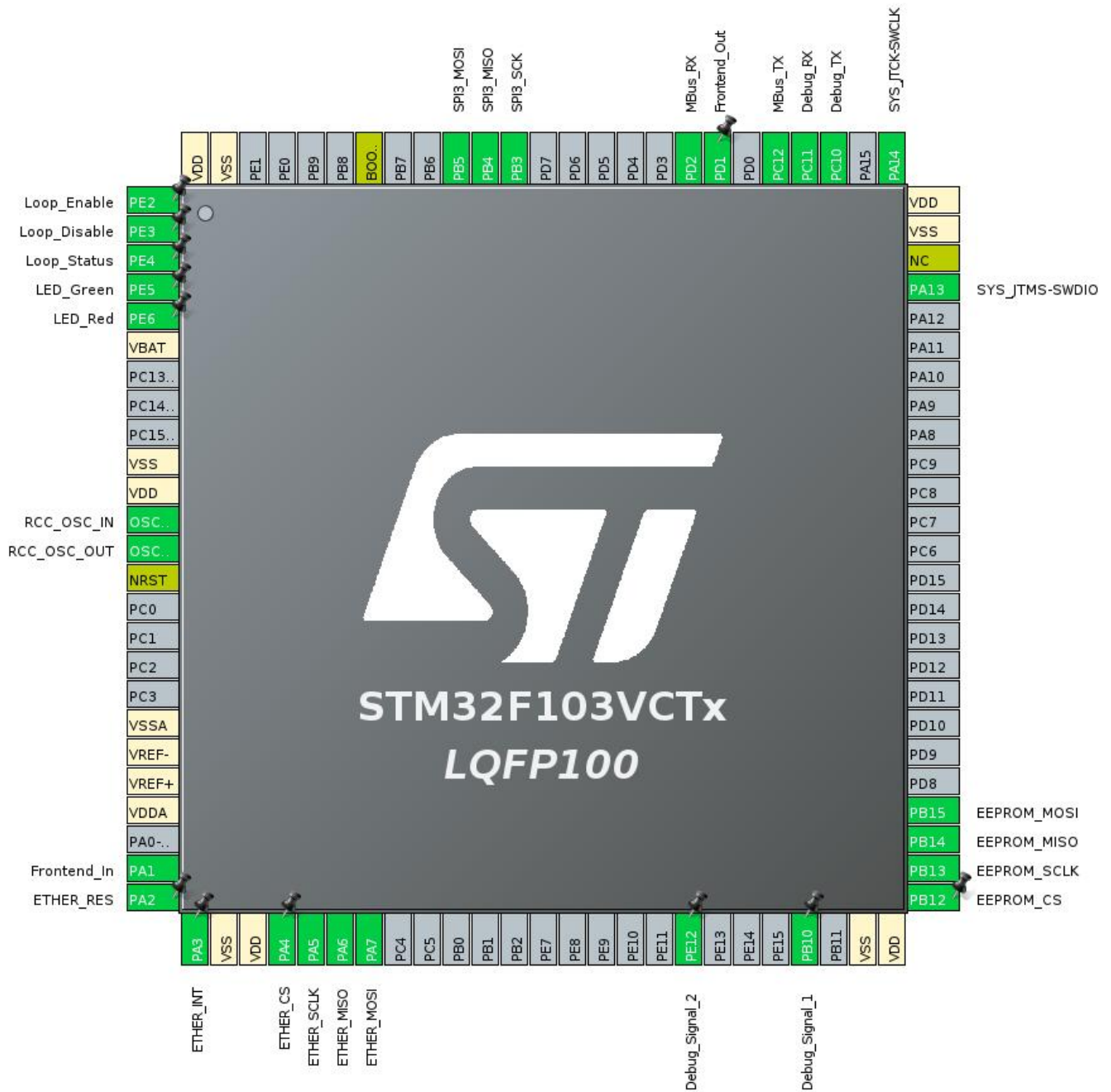
### 1.2. MCU

MCU Series	STM32F1
MCU Line	STM32F103
MCU name	STM32F103VCTx
MCU Package	LQFP100
MCU Pin number	100

### 1.3. Core(s) information

Core(s)	Arm Cortex-M3
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## 2. Pinout Configuration



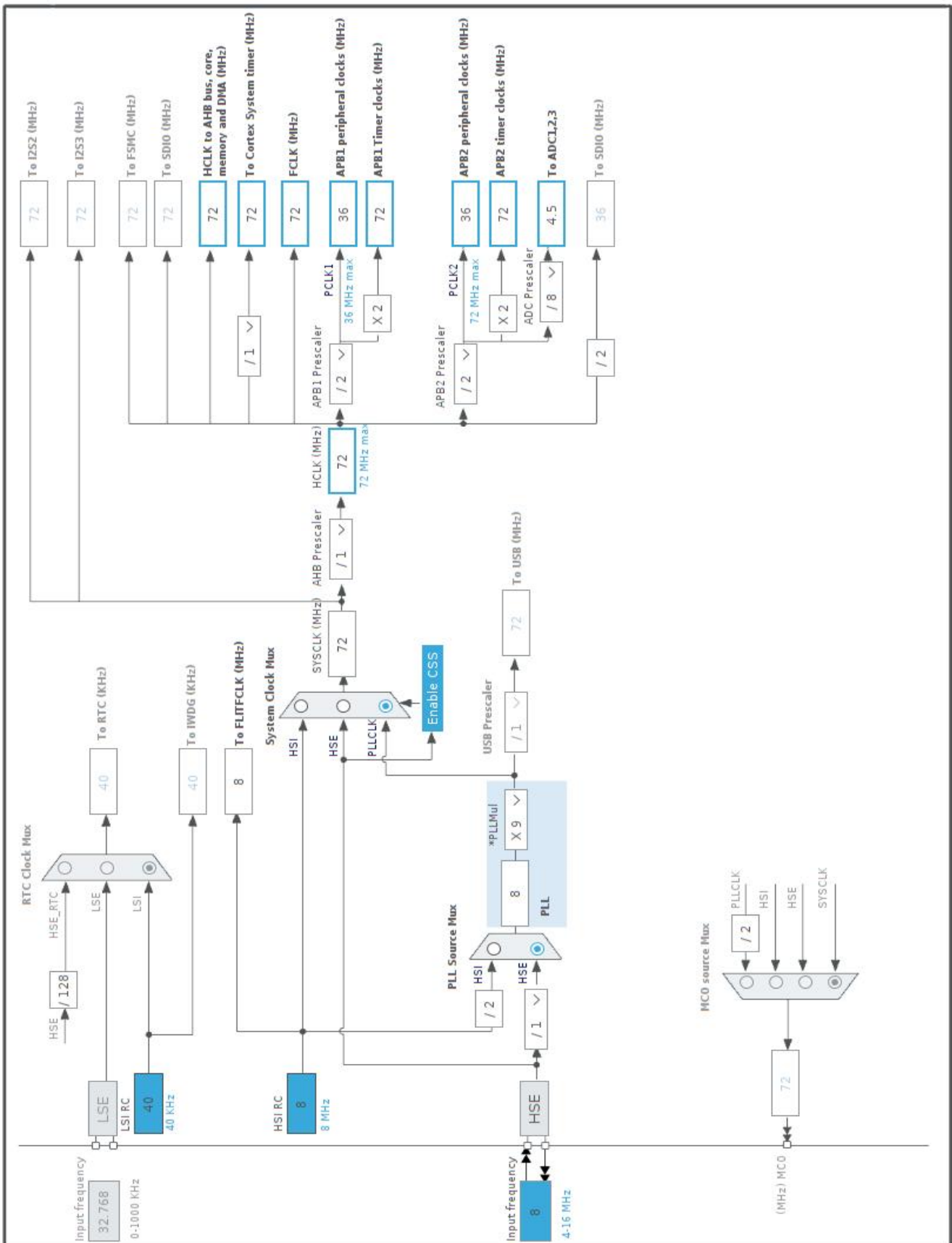
### 3. Pins Configuration

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	PE2 *	I/O	GPIO_Output	Loop_Enable
2	PE3 *	I/O	GPIO_Output	Loop_Disable
3	PE4	I/O	GPIO_EXTI4	Loop_Status
4	PE5 *	I/O	GPIO_Output	LED_Green
5	PE6 *	I/O	GPIO_Output	LED_Red
6	VBAT	Power		
10	VSS	Power		
11	VDD	Power		
12	OSC_IN	I/O	RCC_OSC_IN	
13	OSC_OUT	I/O	RCC_OSC_OUT	
14	NRST	Reset		
19	VSSA	Power		
20	VREF-	Power		
21	VREF+	Power		
22	VDDA	Power		
24	PA1	I/O	ADC1_IN1	Frontend_In
25	PA2 *	I/O	GPIO_Output	ETHER_RES
26	PA3	I/O	GPIO_EXTI3	ETHER_INT
27	VSS	Power		
28	VDD	Power		
29	PA4 *	I/O	GPIO_Output	ETHER_CS
30	PA5	I/O	SPI1_SCK	ETHER_SCLK
31	PA6	I/O	SPI1_MISO	ETHER_MISO
32	PA7	I/O	SPI1_MOSI	ETHER_MOSI
43	PE12 *	I/O	GPIO_Output	Debug_Signal_2
47	PB10 *	I/O	GPIO_Output	Debug_Signal_1
49	VSS	Power		
50	VDD	Power		
51	PB12 *	I/O	GPIO_Output	EEPROM_CS
52	PB13	I/O	SPI2_SCK	EEPROM_SCLK
53	PB14	I/O	SPI2_MISO	EEPROM_MISO
54	PB15	I/O	SPI2_MOSI	EEPROM_MOSI
72	PA13	I/O	SYS_JTMS-SWDIO	
73	NC	NC		
74	VSS	Power		
75	VDD	Power		

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
76	PA14	I/O	SYS_JTCK-SWCLK	
78	PC10	I/O	UART4_TX	Debug_TX
79	PC11	I/O	UART4_RX	Debug_RX
80	PC12	I/O	UART5_TX	MBus_TX
82	PD1 *	I/O	GPIO_Output	Frontend_Out
83	PD2	I/O	UART5_RX	MBus_RX
89	PB3	I/O	SPI3_SCK	
90	PB4	I/O	SPI3_MISO	
91	PB5	I/O	SPI3_MOSI	
94	BOOT0	Boot		
99	VSS	Power		
100	VDD	Power		

\* The pin is affected with an I/O function

## 4. Clock Tree Configuration



## 5. Software Project

### 5.1. Project Settings

Name	Value
Project Name	cube
Project Folder	/home/wn/Workspaces/mbusgateway3variant/cube
Toolchain / IDE	Makefile
Firmware Package Name and Version	STM32Cube FW_F1 V1.8.2
Application Structure	Advanced
Generate Under Root	No
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

### 5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Keep User Code when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

### 5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	IP Instance Name
1	MX_GPIO_Init	GPIO
2	SystemClock_Config	RCC
3	MX_ADC1_Init	ADC1
4	MX_SPI2_Init	SPI2
5	MX_SPI3_Init	SPI3
6	MX_UART4_Init	UART4
7	MX_UART5_Init	UART5
8	MX_SPI1_Init	SPI1

## 6. Power Consumption Calculator report

### 6.1. Microcontroller Selection

Series	STM32F1
Line	STM32F103
MCU	STM32F103VCTx
Datasheet	DS5792_Rev12

### 6.2. Parameter Selection

Temperature	25
Vdd	3.3

### 6.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1



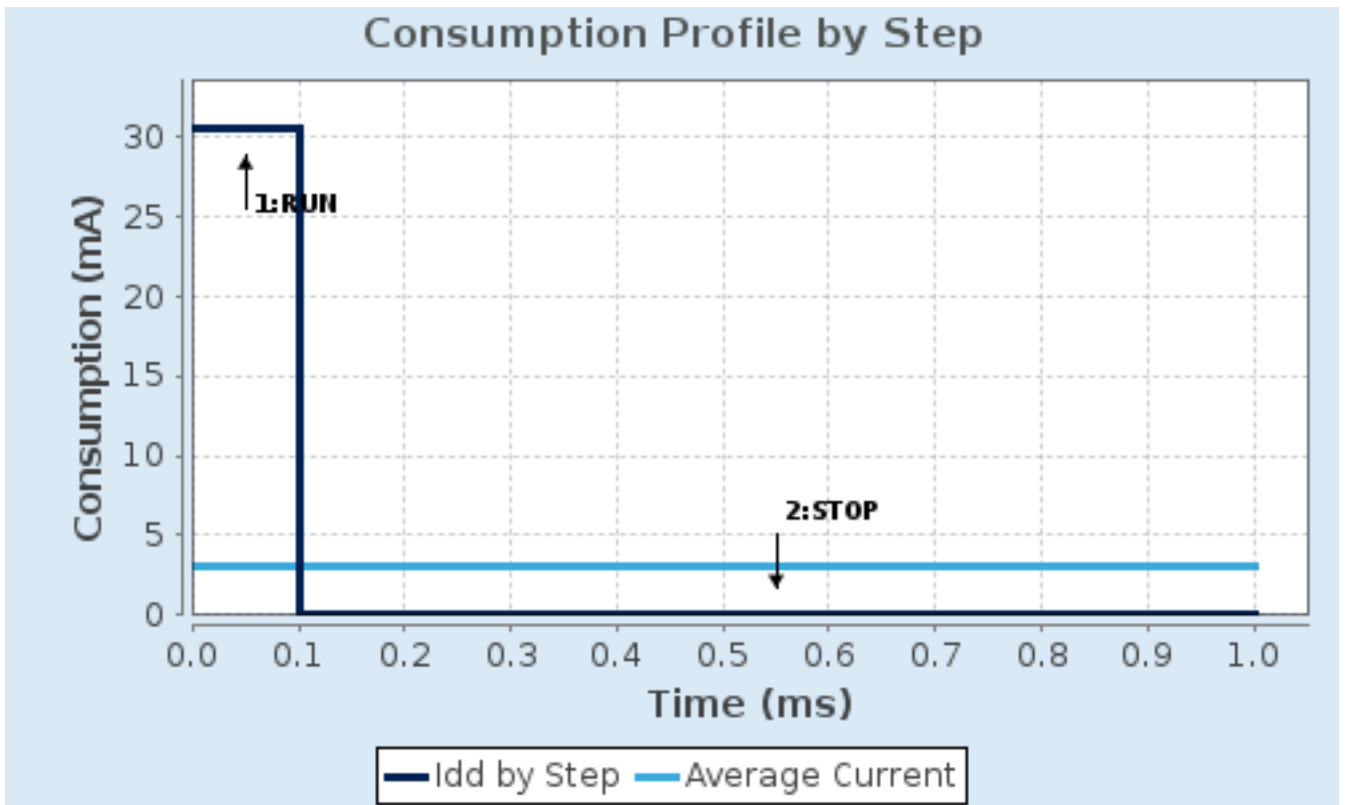
#### 6.4. Sequence

<b>Step</b>	Step1	Step2
<b>Mode</b>	RUN	STOP
<b>Vdd</b>	3.3	3.3
<b>Voltage Source</b>	Battery	Battery
<b>Range</b>	No Scale	No Scale
<b>Fetch Type</b>	FLASH	n/a
<b>CPU Frequency</b>	72 MHz	0 Hz
<b>Clock Configuration</b>	HSE PLL	Regulator LP
<b>Clock Source Frequency</b>	8 MHz	0 Hz
<b>Peripherals</b>		
<b>Additional Cons.</b>	0 mA	0 mA
<b>Average Current</b>	30.5 mA	25 $\mu$ A
<b>Duration</b>	0.1 ms	0.9 ms
<b>DMIPS</b>	90.0	0.0
<b>Ta Max</b>	100.37	105
<b>Category</b>	In DS Table	In DS Table

#### 6.5. Results

Sequence Time	1 ms	Average Current	3.07 mA
Battery Life	1 month, 15 days, 15 hours	Average DMIPS	61.0 DMIPS

#### 6.6. Chart



## 7. IPs and Middleware Configuration

### 7.1. ADC1

**mode: IN1**

#### 7.1.1. Parameter Settings:

##### **ADCs\_Common\_Settings:**

Mode Independent mode

##### **ADC\_Settings:**

Data Alignment Right alignment

Scan Conversion Mode Disabled

Continuous Conversion Mode **Enabled \***

Discontinuous Conversion Mode Disabled

##### **ADC\_Regular\_ConversionMode:**

Enable Regular Conversions Enable

Number Of Conversion 1

External Trigger Conversion Source Regular Conversion launched by software

Rank 1

Channel Channel 1

Sampling Time **71.5 Cycles \***

##### **ADC\_Injected\_ConversionMode:**

Enable Injected Conversions Disable

##### **WatchDog:**

Enable Analog WatchDog Mode false

### 7.2. GPIO

### 7.3. RCC

#### **High Speed Clock (HSE): Crystal/Ceramic Resonator**

#### 7.3.1. Parameter Settings:

##### **System Parameters:**

VDD voltage (V) 3.3

Prefetch Buffer Enabled

Flash Latency(WS) 2 WS (3 CPU cycle)

##### **RCC Parameters:**

HSI Calibration Value 16

HSE Startup Timeout Value (ms) 100

LSE Startup Timeout Value (ms) 5000

## 7.4. SPI1

### Mode: Full-Duplex Master

#### 7.4.1. Parameter Settings:

##### Basic Parameters:

Frame Format Motorola  
Data Size 8 Bits  
First Bit MSB First

##### Clock Parameters:

Prescaler (for Baud Rate) 2  
Baud Rate **18.0 MBits/s \***  
Clock Polarity (CPOL) Low  
Clock Phase (CPHA) 1 Edge

##### Advanced Parameters:

CRC Calculation Disabled  
NSS Signal Type Software

## 7.5. SPI2

### Mode: Full-Duplex Master

#### 7.5.1. Parameter Settings:

##### Basic Parameters:

Frame Format Motorola  
Data Size 8 Bits  
First Bit MSB First

##### Clock Parameters:

Prescaler (for Baud Rate) **4 \***  
Baud Rate **9.0 MBits/s \***  
Clock Polarity (CPOL) Low  
Clock Phase (CPHA) 1 Edge

##### Advanced Parameters:

CRC Calculation Disabled  
NSS Signal Type Software

## 7.6. SPI3

### Mode: Full-Duplex Master

#### 7.6.1. Parameter Settings:

##### Basic Parameters:

Frame Format	Motorola
Data Size	8 Bits
First Bit	MSB First

##### Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	<b>18.0 MBits/s *</b>
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

##### Advanced Parameters:

CRC Calculation	Disabled
NSS Signal Type	Software

## 7.7. SYS

### Debug: Serial Wire

### Timebase Source: SysTick

## 7.8. UART4

### Mode: Asynchronous

#### 7.8.1. Parameter Settings:

##### Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

##### Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

## 7.9. UART5

**Mode: Asynchronous**

### 7.9.1. Parameter Settings:

**Basic Parameters:**

Baud Rate	<b>2400 *</b>
Word Length	<b>9 Bits (including Parity) *</b>
Parity	<b>Even *</b>
Stop Bits	1

**Advanced Parameters:**

Data Direction	Receive and Transmit
Over Sampling	16 Samples

\* **User modified value**

## 8. System Configuration

### 8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA1	ADC1_IN1	Analog mode	n/a	n/a	Frontend_In
RCC	OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SPI1	PA5	SPI1_SCK	Alternate Function Push Pull	n/a	High *	ETHER_SCLK
	PA6	SPI1_MISO	Input mode	No pull-up and no pull-down	n/a	ETHER_MISO
	PA7	SPI1_MOSI	Alternate Function Push Pull	n/a	High *	ETHER_MOSI
SPI2	PB13	SPI2_SCK	Alternate Function Push Pull	n/a	High *	EEPROM_SCLK
	PB14	SPI2_MISO	Input mode	No pull-up and no pull-down	n/a	EEPROM_MISO
	PB15	SPI2_MOSI	Alternate Function Push Pull	n/a	High *	EEPROM_MOSI
SPI3	PB3	SPI3_SCK	Alternate Function Push Pull	n/a	High *	
	PB4	SPI3_MISO	Input mode	No pull-up and no pull-down	n/a	
	PB5	SPI3_MOSI	Alternate Function Push Pull	n/a	High *	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
UART4	PC10	UART4_TX	Alternate Function Push Pull	n/a	High *	Debug_TX
	PC11	UART4_RX	Input mode	No pull-up and no pull-down	n/a	Debug_RX
UART5	PC12	UART5_TX	Alternate Function Push Pull	n/a	High *	MBus_TX
	PD2	UART5_RX	Input mode	No pull-up and no pull-down	n/a	MBus_RX
GPIO	PE2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Loop_Enable
	PE3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Loop_Disable
	PE4	GPIO_EXTI4	<b>External Interrupt Mode with Rising/Falling edge</b>	<b>Pull-up *</b>	n/a	Loop_Status
	PE5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_Green
	PE6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED_Red
	PA2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	ETHER_RES
	PA3	GPIO_EXTI3	External Interrupt Mode with Rising edge trigger detection	No pull-up and no pull-down	n/a	ETHER_INT
	PA4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	ETHER_CS
	PE12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Debug_Signal_2
	PB10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Debug_Signal_1
	PB12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	EEPROM_CS

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PD1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Frontend_Out

## 8.2. DMA configuration

nothing configured in DMA service



### 8.3. NVIC configuration

#### 8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Prefetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
EXTI line4 interrupt	true	0	0
ADC1 and ADC2 global interrupts	true	0	0
SPI2 global interrupt	true	0	0
UART4 global interrupt	true	0	0
UART5 global interrupt	true	0	0
PVD interrupt through EXTI line 16		unused	
Flash global interrupt		unused	
RCC global interrupt		unused	
EXTI line3 interrupt		unused	
SPI1 global interrupt		unused	
SPI3 global interrupt		unused	

#### 8.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	true	true	false
Hard fault interrupt	true	true	false
Memory management fault	true	true	false
Prefetch fault, memory access fault	true	true	false
Undefined instruction or illegal state	true	true	false
System service call via SWI instruction	true	true	false
Debug monitor	true	true	false
Pendable request for system service	true	true	false
System tick timer	true	true	true
EXTI line4 interrupt	true	true	true
ADC1 and ADC2 global interrupts	true	true	true
SPI2 global interrupt	true	true	true
UART4 global interrupt	true	true	true

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
UART5 global interrupt	true	true	true

\* User modified value

## 9. System Views

### 9.1. Category view

#### 9.1.1. Current

#### Middleware

#### System Core

#### Analog

#### Timers

#### Connectivity

#### Multimedia

#### Computing

DMA

ADC1 

SPI1 

GPIO 

SPI2 

NVIC 

SPI3 

RCC 

UART4 

SYS 

UART5 

## 10. Docs & Resources

Type	Link
Datasheet	<a href="http://www.st.com/resource/en/datasheet/CD00191185.pdf">http://www.st.com/resource/en/datasheet/CD00191185.pdf</a>
Reference manual	<a href="http://www.st.com/resource/en/reference_manual/CD00171190.pdf">http://www.st.com/resource/en/reference_manual/CD00171190.pdf</a>
Programming manual	<a href="http://www.st.com/resource/en/programming_manual/CD00228163.pdf">http://www.st.com/resource/en/programming_manual/CD00228163.pdf</a>
Programming manual	<a href="http://www.st.com/resource/en/programming_manual/CD00283419.pdf">http://www.st.com/resource/en/programming_manual/CD00283419.pdf</a>
Errata sheet	<a href="http://www.st.com/resource/en/errata_sheet/CD00197763.pdf">http://www.st.com/resource/en/errata_sheet/CD00197763.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/CD00160362.pdf">http://www.st.com/resource/en/application_note/CD00160362.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/CD00164185.pdf">http://www.st.com/resource/en/application_note/CD00164185.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/CD00167594.pdf">http://www.st.com/resource/en/application_note/CD00167594.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/CD00200423.pdf">http://www.st.com/resource/en/application_note/CD00200423.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/CD00211314.pdf">http://www.st.com/resource/en/application_note/CD00211314.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/CD00249778.pdf">http://www.st.com/resource/en/application_note/CD00249778.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/CD00259245.pdf">http://www.st.com/resource/en/application_note/CD00259245.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/CD00264321.pdf">http://www.st.com/resource/en/application_note/CD00264321.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/CD00264342.pdf">http://www.st.com/resource/en/application_note/CD00264342.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/CD00264379.pdf">http://www.st.com/resource/en/application_note/CD00264379.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/DM00024853.pdf">http://www.st.com/resource/en/application_note/DM00024853.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/DM00032987.pdf">http://www.st.com/resource/en/application_note/DM00032987.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/DM00033267.pdf">http://www.st.com/resource/en/application_note/DM00033267.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/DM00033344.pdf">http://www.st.com/resource/en/application_note/DM00033344.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/DM00042534.pdf">http://www.st.com/resource/en/application_note/DM00042534.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/DM00052530.pdf">http://www.st.com/resource/en/application_note/DM00052530.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/DM00073742.pdf">http://www.st.com/resource/en/application_note/DM00073742.pdf</a>
Application note	<a href="http://www.st.com/resource/en/application_note/DM00080497.pdf">http://www.st.com/resource/en/application_note/DM00080497.pdf</a>
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Application note [http://www.st.com/resource/en/application\\_note/DM00160482.pdf](http://www.st.com/resource/en/application_note/DM00160482.pdf)  
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Application note [http://www.st.com/resource/en/application\\_note/DM00236305.pdf](http://www.st.com/resource/en/application_note/DM00236305.pdf)  
Application note [http://www.st.com/resource/en/application\\_note/DM00296349.pdf](http://www.st.com/resource/en/application_note/DM00296349.pdf)  
Application note [http://www.st.com/resource/en/application\\_note/DM00325582.pdf](http://www.st.com/resource/en/application_note/DM00325582.pdf)  
Application note [http://www.st.com/resource/en/application\\_note/DM00327191.pdf](http://www.st.com/resource/en/application_note/DM00327191.pdf)  
Application note [http://www.st.com/resource/en/application\\_note/DM00354244.pdf](http://www.st.com/resource/en/application_note/DM00354244.pdf)  
Application note [http://www.st.com/resource/en/application\\_note/DM00315319.pdf](http://www.st.com/resource/en/application_note/DM00315319.pdf)  
Application note [http://www.st.com/resource/en/application\\_note/DM00380469.pdf](http://www.st.com/resource/en/application_note/DM00380469.pdf)  
Application note [http://www.st.com/resource/en/application\\_note/DM00395696.pdf](http://www.st.com/resource/en/application_note/DM00395696.pdf)  
Application note [http://www.st.com/resource/en/application\\_note/DM00493651.pdf](http://www.st.com/resource/en/application_note/DM00493651.pdf)  
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