1. Description

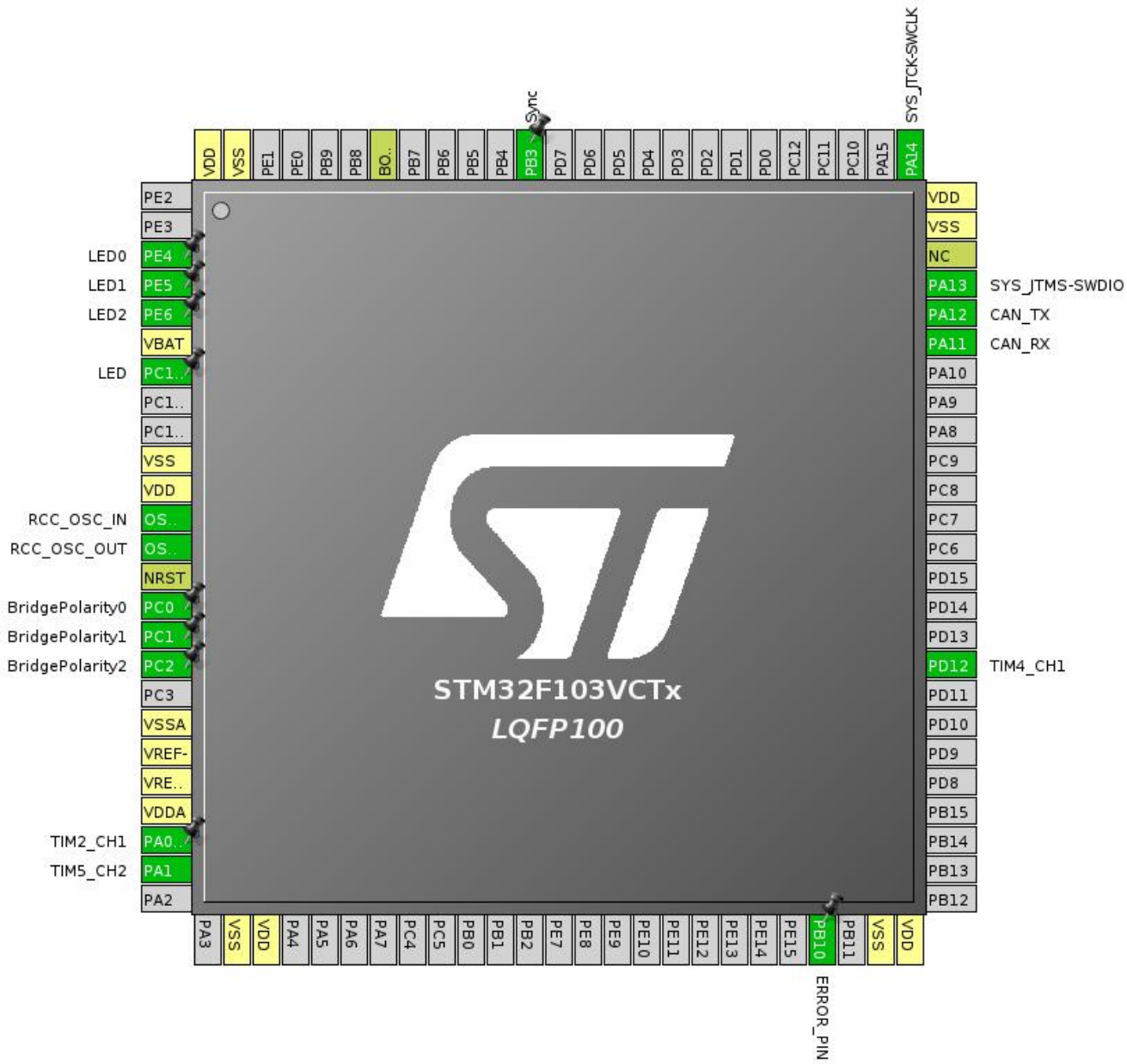
1.1. Project

Project Name	inverter2
Board Name	inverter2
Generated with:	STM32CubeMX 4.16.1
Date	10/26/2016

1.2. MCU

MCU Series	STM32F1
MCU Line	STM32F103
MCU name	STM32F103VCTx
MCU Package	LQFP100
MCU Pin number	100

2. Pinout Configuration

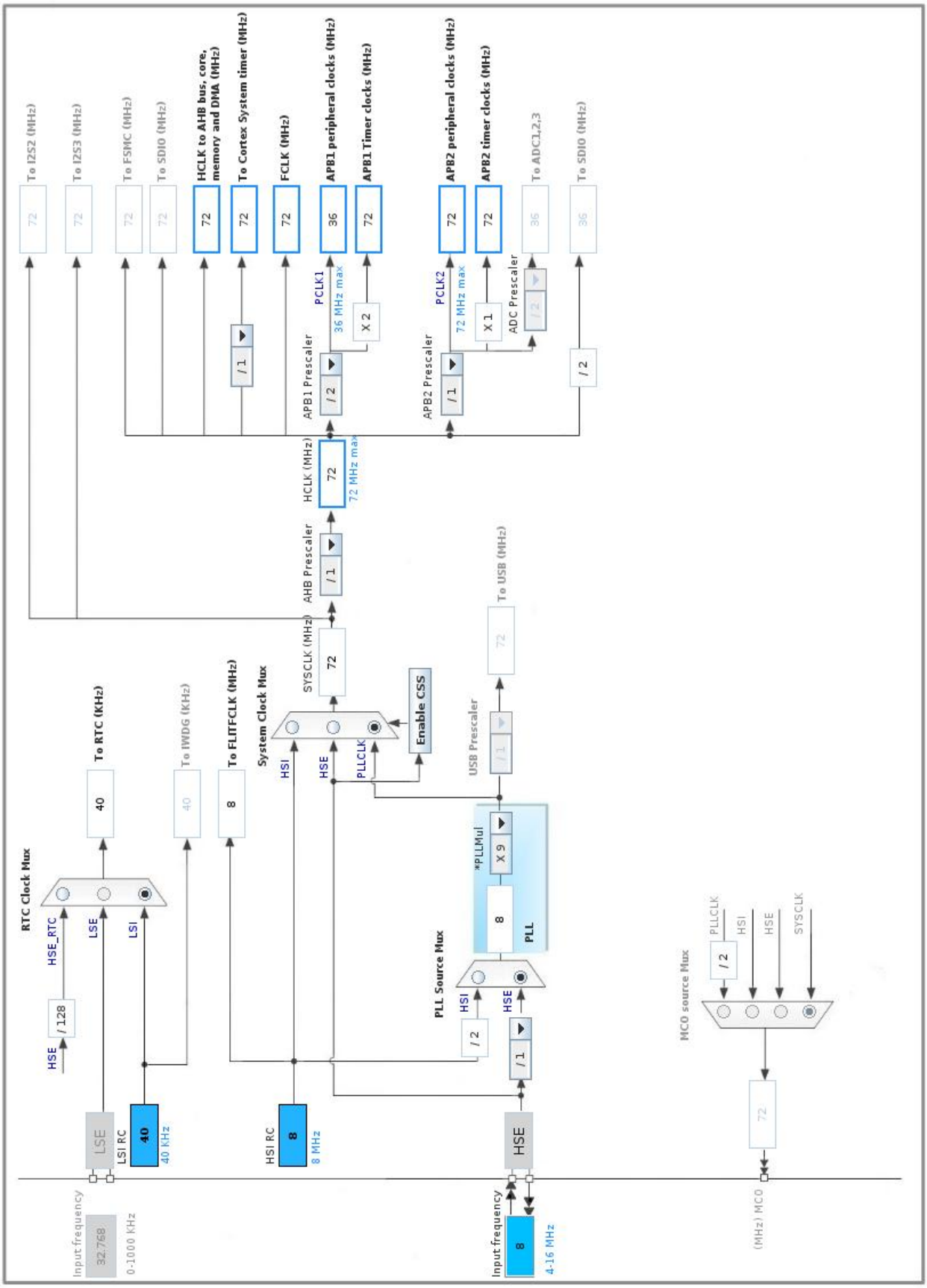


3. Pins Configuration

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
3	PE4 *	I/O	GPIO_Output	LED0
4	PE5 *	I/O	GPIO_Output	LED1
5	PE6 *	I/O	GPIO_Output	LED2
6	VBAT	Power		
7	PC13-TAMPER-RTC *	I/O	GPIO_Output	LED
10	VSS	Power		
11	VDD	Power		
12	OSC_IN	I/O	RCC_OSC_IN	
13	OSC_OUT	I/O	RCC_OSC_OUT	
14	NRST	Reset		
15	PC0 *	I/O	GPIO_Output	BridgePolarity0
16	PC1 *	I/O	GPIO_Output	BridgePolarity1
17	PC2 *	I/O	GPIO_Output	BridgePolarity2
19	VSSA	Power		
20	VREF-	Power		
21	VREF+	Power		
22	VDDA	Power		
23	PA0-WKUP	I/O	TIM2_CH1	
24	PA1	I/O	TIM5_CH2	
27	VSS	Power		
28	VDD	Power		
47	PB10 *	I/O	GPIO_Output	ERROR_PIN
49	VSS	Power		
50	VDD	Power		
59	PD12	I/O	TIM4_CH1	
70	PA11	I/O	CAN_RX	
71	PA12	I/O	CAN_TX	
72	PA13	I/O	SYS_JTMS-SWDIO	
73	NC	NC		
74	VSS	Power		
75	VDD	Power		
76	PA14	I/O	SYS_JTCK-SWCLK	
89	PB3 *	I/O	GPIO_Output	Sync
94	BOOT0	Boot		
99	VSS	Power		
100	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. IPs and Middleware Configuration

5.1. CAN

mode: Mode

5.1.1. Parameter Settings:

Bit Timings Parameters:

Prescaler (for Time Quantum)	16
Time Quantum	**444.44444444444446 ***
Time Quanta in Bit Segment 1	1 Time
Time Quanta in Bit Segment 2	1 Time
Time for one Bit	**1333 ***
ReSynchronization Jump Width	1 Time

Basic Parameters:

Time Triggered Communication Mode	Disable
Automatic Bus-Off Management	Disable
Automatic Wake-Up Mode	Disable
No-Automatic Retransmission	Disable
Receive Fifo Locked Mode	Disable
Transmit Fifo Priority	Disable

Advanced Parameters:

Operating Mode	Normal

5.2. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

5.2.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Prefetch Buffer	Enabled
Flash Latency(WS)	2 WS (3 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
HSE Startup Timout Value (ms)	100

LSE Startup Timout Value (ms)	5000

5.3. RTC

RTC OUT: No RTC Output

5.3.1. Parameter Settings:

General:

Auto Predivider Calculation	Enabled
Asynchronous Predivider value	Automatic Predivider Calculation Enabled
Output	No output on the TAMPER pin

Calendar Time:

Data Format	**Binary data format ***
Hours	1
Minutes	0
Seconds	0

Calendar Date:

Week Day	Monday
Month	January
Date	1
Year	0

5.4. SYS

Debug: Serial Wire

Timebase Source: SysTick

5.5. TIM1

Clock Source : Internal Clock

5.5.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**72 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**5000 ***

Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

5.6. TIM2

Clock Source : Internal Clock

Channel1: PWM Generation CH1

5.6.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**72 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**5000 ***
Internal Clock Division (CKD)	No Division

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	**1000 ***
Fast Mode	Disable
CH Polarity	High

5.7. TIM4

Clock Source : Internal Clock

Channel1: PWM Generation CH1

5.7.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**72 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	

	5000 *
Internal Clock Division (CKD)	No Division

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High

5.8. TIM5

mode: Clock Source

Channel2: PWM Generation CH2

5.8.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**72 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**5000 ***
Internal Clock Division (CKD)	No Division

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High

*** User modified value**

6. System Configuration

6.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
CAN	PA11	CAN_RX	Input mode	No pull-up and no pull-down	n/a	
	PA12	CAN_TX	Alternate Function Push Pull	n/a	**High ***	
RCC	OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
TIM2	PA0-WKUP	TIM2_CH1	Alternate Function Push Pull	n/a	Low	
TIM4	PD12	TIM4_CH1	Alternate Function Push Pull	n/a	Low	
TIM5	PA1	TIM5_CH2	Alternate Function Push Pull	n/a	Low	
GPIO	PE4	GPIO_Output	Output Push Pull	n/a	Low	LED0
	PE5	GPIO_Output	Output Push Pull	n/a	Low	LED1
	PE6	GPIO_Output	Output Push Pull	n/a	Low	LED2
	PC13-TAMPER-RTC	GPIO_Output	Output Push Pull	n/a	Low	LED
	PC0	GPIO_Output	Output Push Pull	n/a	Low	BridgePolarity0
	PC1	GPIO_Output	Output Push Pull	n/a	Low	BridgePolarity1
	PC2	GPIO_Output	Output Push Pull	n/a	Low	BridgePolarity2
	PB10	GPIO_Output	Output Push Pull	n/a	Low	ERROR_PIN
	PB3	GPIO_Output	Output Push Pull	n/a	Low	Sync

6.2. DMA configuration

DMA request	Stream	Direction	Priority
TIM4_CH1	DMA1_Channel1	Memory To Peripheral	Low
TIM5_CH2	DMA2_Channel4	Memory To Peripheral	Low
TIM2_CH1	DMA1_Channel5	Memory To Peripheral	Low

TIM4_CH1: DMA1_Channel1 DMA request Settings:

Mode: **Circular ***
Peripheral Increment: Disable
Memory Increment: **Enable ***
Peripheral Data Width: Half Word
Memory Data Width: Half Word

TIM5_CH2: DMA2_Channel4 DMA request Settings:

Mode: **Circular ***
Peripheral Increment: Disable
Memory Increment: **Enable ***
Peripheral Data Width: Half Word
Memory Data Width: Half Word

TIM2_CH1: DMA1_Channel5 DMA request Settings:

Mode: **Circular ***
Peripheral Increment: Disable
Memory Increment: **Enable ***
Peripheral Data Width: Half Word
Memory Data Width: Half Word

6.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Prefetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
DMA1 channel1 global interrupt	true	0	0
DMA1 channel5 global interrupt	true	0	0
TIM1 update interrupt	true	0	0
TIM2 global interrupt	true	0	0
TIM4 global interrupt	true	0	0
TIM5 global interrupt	true	0	0
DMA2 channel4 and channel5 global interrupts	true	0	0
PVD interrupt through EXTI line 16	unused		
RTC global interrupt	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
USB high priority or CAN TX interrupts	unused		
USB low priority or CAN RX0 interrupts	unused		
CAN RX1 interrupt	unused		
CAN SCE interrupt	unused		
TIM1 break interrupt	unused		
TIM1 trigger and commutation interrupts	unused		
TIM1 capture compare interrupt	unused		
RTC alarm interrupt through EXTI line 17	unused		

*** User modified value**

7. Power Consumption Calculator report

7.1. Microcontroller Selection

Series	STM32F1
Line	STM32F103
MCU	STM32F103VCTx
Datasheet	14611_Rev12

7.2. Parameter Selection

Temperature	25
Vdd	3.3

8. Software Project

8.1. Project Settings

Name	Value
Project Name	inverter2
Project Folder	/home/wn/workspace-stm32/inverter2/cubemx/output/inverter2
Toolchain / IDE	SW4STM32
Firmware Package Name and Version	STM32Cube FW_F1 V1.4.0

8.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No